Battery Management Systems for Electric Vehicle Applications

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Abstract

A high-voltage gain SEPIC DC-DC converter powers a BLDC motor-based pumping system, enabling efficient operation in conditions of mixed load and constant speed. Three single-phase, two-module interleaved isolated SEPIC converters with parallel output connections are also advised for an ultra-fast EV charger. The architecture ensures modularity, fault ride-through capability, and redundancy, significantly enhancing system reliability. MATLAB/Simulink simulations validate the system's performance in minimizing torque ripple, reducing speed error, and improving dynamic response. Additionally, power quality is improved through enhanced power factor, harmonic reduction, and tightly regulated DC output voltage. These characteristics make the system highly suitable for reliable and cost-effective deployment in electric vehicle charging and pumping applications.

Keywords: BLDC motor, SEPIC converter, interleaved topology, EV charging, power quality, torque ripple minimization, fault tolerance, MATLAB/Simulink.

I. INTRODUCTION

Brushless DC (BLDC) motors' high efficiency, small design, and exceptional torque characteristics have made them more popular in applications including electric vehicles (EVs), water pumping systems, and renewable energy sets. [1], [2]. Their integration with advanced power electronic converters enhances system performance, particularly in scenarios demanding precise control and energy efficiency.

The ability to convert voltages both up and down while maintaining a non-inverting output makes the Single-Ended Primary Inductor Converter (SEPIC) special among DC-DC converters[3]. This versatility makes SEPIC converters suitable for applications like photovoltaic (PV) systems and battery-powered devices, where input voltages can vary

significantly [4]. In PV-fed water pumping systems, employing a SEPIC converter can optimize the power extraction from solar panels, ensuring consistent motor operation despite fluctuating solar irradiance [5].

Interleaving multiple SEPIC converters can further enhance system performance by reducing input and output current ripples, improving thermal distribution, and increasing overall efficiency [6]. Such configurations are particularly beneficial in high-power applications like ultra-fast EV charging, where reliability and efficiency are paramount [7]. The modular nature of interleaved converters also facilitates scalability and fault tolerance, essential features for modern EV charging infrastructure [8].

Torque ripple in BLDC motors is a critical concern, as it can lead to mechanical vibrations, acoustic noise, and reduced lifespan of mechanical components [9]. To reduce torque ripple and improve motor performance, sophisticated control techniques including Field-Oriented Control (FOC) and Space Vector Modulation (SVM) have been developed. [10], [11]. Simulation tools like MATLAB/Simulink are crucial for developing and validating these control strategies as well as analyzing the system's behaviour under various operating situations. [12].

Recent studies have demonstrated the effectiveness of integrating SEPIC converters with BLDC motor drives in improving system efficiency and performance. For instance, incorporating a SEPIC converter in a PV-fed BLDC motor drive system has shown significant improvements in power factor correction and harmonic reduction [13]. Similarly, the use of interleaved SEPIC converters in EV charging stations has led to enhanced charging speeds and better thermal management [14].

Building on previous developments, this paper suggests a complete system that includes an ultra-fast EV charger employing interleaved SEPIC modules, a BLDC motor-driven pumping mechanism, and a high-voltage gain SEPIC DC-DC converter [15]-[19]. The system aims to achieve improved power quality, reduced torque ripple, and enhanced reliability [20]-[22]. Simulation studies conducted using MATLAB/Simulink validate the proposed system's performance, demonstrating its suitability for both water pumping and EV charging applications [23]-[24].

II. SYSTEM DESCRIPTION

The proposed approach uses a unidirectional converter with a full diode-bridge in the first stage of the converter. The second stage involves creating an isolated and interleaved version of the fundamental SEPIC DC–DC converter, as shown in Figure 1. DICM and DCVM are both part of DCM operation. DICM is considered in the output inductance (the magnetizing inductance of the HFT) as long as the battery side current stays constant.

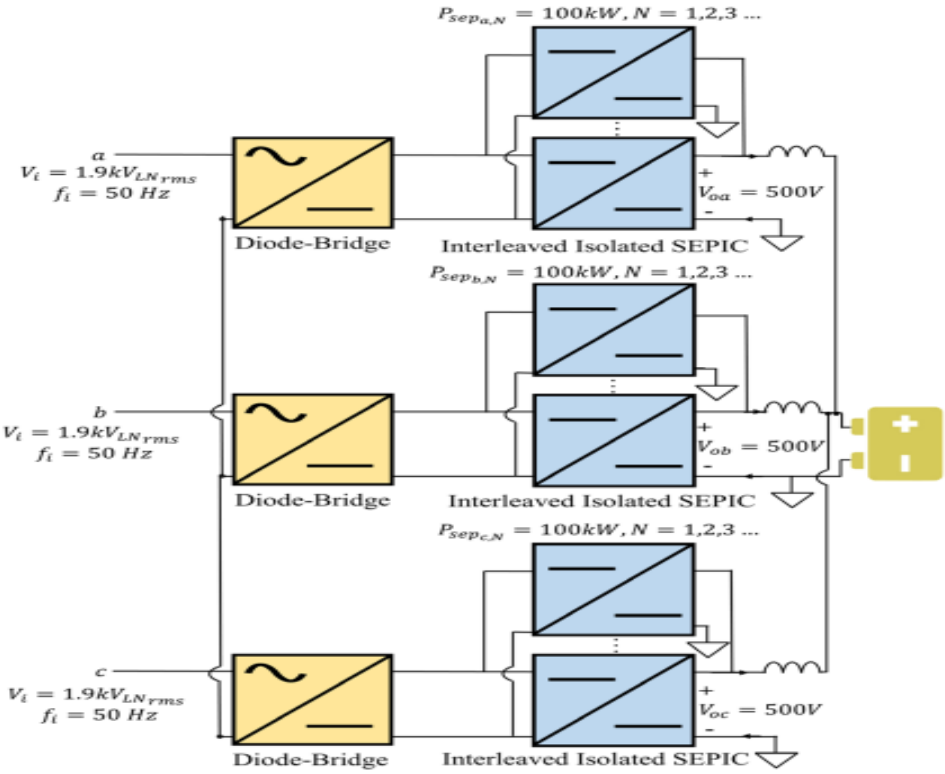

Figure 1: Block diagram of phase-modular interleaved isolated SEPIC DC–DC converter

The SEPIC's intermediate capacitor considers DCVM operation. Due to the increased voltage stress on the switch, DCVM operation is not advised for high-power systems. For low power modules that can be integrated to handle higher power per phase and connected in parallel, interleaving is used to enable DCM operation. The output of every phase in the suggested system is connected in parallel, as seen in Figure 2. HFTs can be used to separate the input and output sides, which is necessary for the parallel connection of the output side.

A. Circuit Operation

Figure 2 illustrates the analogous circuit to which the main side of the HFT is referred to by the transformer's turns ratio n (= Vs⁄Vp). The output current is stated using KCL as follows:

$$i'_{oa} + i'_{ob} + i'_{oc} = i'_o = ni_o$$

$$\text{where } i'_{ok} = \sum_{i=1}^{N} i'_{oki}, k = a, b, c \tag{1}$$

Depending on the pulse given to the switch, the converter alternates between five modes on a regular basis:

Mode 1:

As seen in Figure 2, the ON time of the PWM signal applied to the semiconductor device determines this mode. If k = a, b, c & N = 1, 2, 3, …, then i_{kN} represents the freewheeling

input current that flows before this phase and is stored in the input inductor. Since the freewheeling current runs in the opposite direction of the current in L2, it is negative; yet, it is positive since it flows in the same direction as the current in Lf. In this mode, KVL can be used to mathematically express the inductor currents.

$$i_{s_k} = i_{fwkN} + \frac{v_{sk}}{L_f} t \text{ for } k = a, b, c \ \& \ N = 1, 2, 3, \ldots \quad (2)$$

$$i_{L2N} = -i_{fwkN} + \frac{|v_{sk}|}{L_{2N}} t \text{ for } k = a, b, c \ \& \ N = 1, 2, 3, \ldots \quad (3)$$

Mode 2:

When the gate signals fall to zero, the switches and diodes in each phase are switched off and on, accordingly. This marks the start of Mode 2. The current flowing through the inductors can be shown using the equivalent circuit of this mode and KCL in Figure 2.

$$i_{s_k} = i_{fwkN} + \frac{v_{sk}}{L_f} dT_s - \frac{v_o}{nL_f} t \quad (4)$$

$$\text{for } k = a, b, c \ \& \ N = 1, 2, 3, \ldots$$

The above equation can be rewritten for inductor current as:

$$i_{L2N} = -i_{fwkN} + \frac{|v_{sk}|}{L_2} dT_s - \frac{v_o}{nL_{2N}} t \quad (5)$$

$$\text{for } k = a, b, c \ \& \ N = 1, 2, 3, \ldots$$

(5) states that the current passing through L2N and, consequently, the magnitude of the phase voltage are proportional to the quantity of energy stored in L2N. By blocking the diode in phase B, this mode is stopped since B contains the least energy, which implies

$$i'_{Db} = 0 \rightarrow \ i_{L_f b} = -i_{L2bN} \text{ for } N = 1, 2, 3 \ldots \quad (6)$$

Thus, the duration of Mode 2 is determined by the diode ON time in phase B. To use (3), (4), and (5) to find the diode's ON time:

$$t_{DbN_{ON}} = \frac{|v_{sb}|}{v_o} n d T_s = d_1 T_s \quad (7)$$

Mode 3:

This mode begins when the phase B diode is blocked and continues until the phase C diode is blocked as well. The diode's ON time in phase C determines how long this mode lasts.

$$i'_{Dc} = 0 \rightarrow i_{Lfb} = -i_{L2cN} \text{ for } N = 1, 2, 3 \ldots \quad (8)$$

Hence

$$t_{DcN\,ON} = \frac{|v_{sc}|}{v_o} nd T_s = d_2 T_s \quad (9)$$

Mode 4:

Similar to Mode 3, this mode begins when the phase C diode is blocked and continues until the phase A diode is blocked. The analogous circuit for this mode. It is possible to obtain a general formula that is given as (8), (9), and (10), which show that, in theory, the ON time is the same for all modules in all phases.

$$t_{DkN\,ON} = \frac{|v_{sk}|}{v_o} nd T_s = d_i T_s \quad (10)$$

where i = 1,2,3 for k = b, c, a respectively.

Mode 5:

This mode is basically the mode where the freewheeling currents continue to flow until the next switching period because all switches and diodes are off due to the extremely large input inductances Ls or L1N. This period's duration can be computed by

$$d_4 T_s = \left(1 - d - \sum_{i=1}^{3} d_i\right) T_s \quad (11)$$

The instantaneous average output current for sector 4 is then integrated to determine the average output current for a line period.

$$I_o = \frac{\pi}{6} \int_{\pi/3}^{\pi/2} i_o(t)\, d(\omega t) = \frac{3NV_p^2 d^2 T_s}{4 v_o L_{eqN}} \quad (12)$$

Each single-phase module in the suggested system can be examined independently to determine whether the system is balanced. Assuming a lossless system, the output power of a single module is equal to its input power in a single phase., that is

$$v_{sk} i_{skN} = v_o I_{okN} \quad (13)$$

Where,

$$i_{skN} = \frac{v_{sk} d^2 T_s}{2 L_{eqN}}$$

$$i_{sk} = \frac{V_p d^2 T_s}{2 L_{eqN}} \sin(\omega t) = I_{Npk} \sin(\omega t)$$

Consequently, the total input current peak to phase k is given by

$$I_{pk} = \sum_{i=1}^{N} I_{ipk} \tag{14}$$

Equation (13), The phase current, which has a peak value INpk and is in-phase with the phase input voltage for k = a, b, and c, demonstrates the unity PF of SEPIC PFC. Low THD is ensured by the input inductances filtering the high order harmonics.

B. Inductor and capacitor Design

The expected ripple in the input current determines the value of the inductor Lf. It supplies the input current as well as its ripple.

$$\Delta i_{sN} = \frac{v_s}{L_f} d T_s \text{ where } i_{sN} = \frac{i_s}{N} \tag{15}$$

The inductor value can be calculated using (15) in the following way: When the voltage is at its highest, the current ripples the most.

$$L_f = \frac{V_p d T_s}{\Delta i_{sN}} \tag{16}$$

The value of the inductance L2N can then be ascertained using (16).

$$L_{2N} = \frac{L_f L_{eqN}}{L_f - L_{eqN}} \tag{17}$$

Where, $L_{eqN} = \frac{R T_s k_{aN}}{2}$

Two requirements should be met by the intermediate capacitor's value: During the switching period, it must maintain a constant capacitor voltage; during the line period, it must follow the input voltage. Furthermore, the resonance frequency induced by C1N, L1N, and L2N should be considered in order to avoid oscillatory behavior at each half cycle of the input current. The line frequency and the switching frequency should be distinguished using the resonant frequency, which is

$$\omega_i < \omega_r < \omega_s$$

Hence, the capacitance value is

$$C_{1N} = \frac{1}{\omega_r{}^2 \left(L_f + L_{2N}\right)} \text{ for } N = 1, 2, 3, \ldots \tag{18}$$

III. CONTROL OF PROPOSED SYSTEM WITH CONVERNTIONAL CONTROL

A. Closed-loop control

The block diagram for the closed-loop control of the entire converter is displayed while employing the Constant Current (CC) charging approach, which supplies a steady current to the EV battery. Since SEPIC in DCM operates like a resistive load, as the study will demonstrate theoretically, only one control loop is required for DCM operation.

Since SEPIC modules will function as parallel resistive loads, this idea remains valid even when they are interleaved.

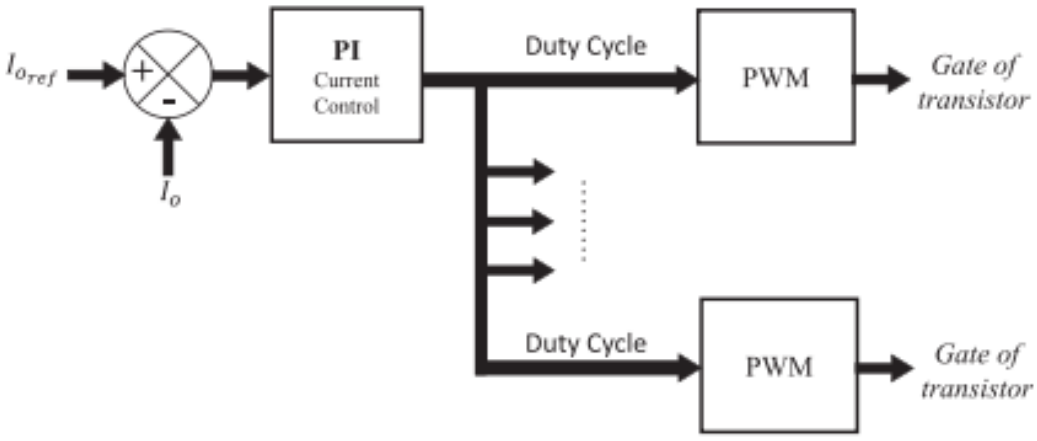

Figure 2:Block diagram of the closed-loop controller for DCM mode (employing CC charging approach)

IV. Results & Discussion

The Simulink Diagram of the proposed system is shown below: Figure 5, represents waveform of stator current and emf of Phase A. Figure 6 represents the rotor speed of BLDC motor. The controller action is evident that it settles at 0.03 seconds with very minimum overshoot of 5%. Figure 7, represents the electromagnetic torque developed by BLDC motor.

The transient portion lass not more the 0.02 sec ,represents controller performance in settling the desired speed and torque with in short interval.

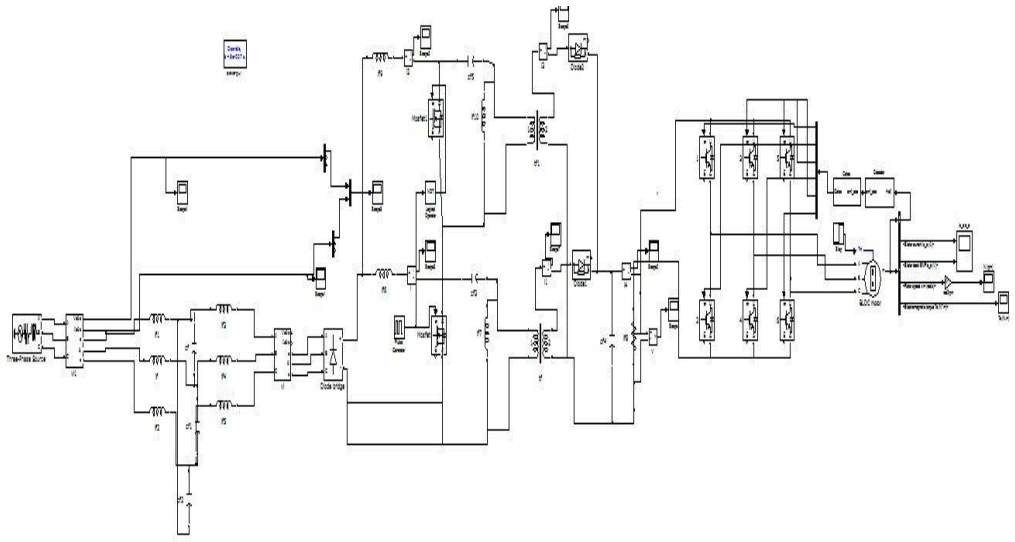

Figure 3:Simulink Diagram of BLDC Motor Drive Fed SEPIC Converter

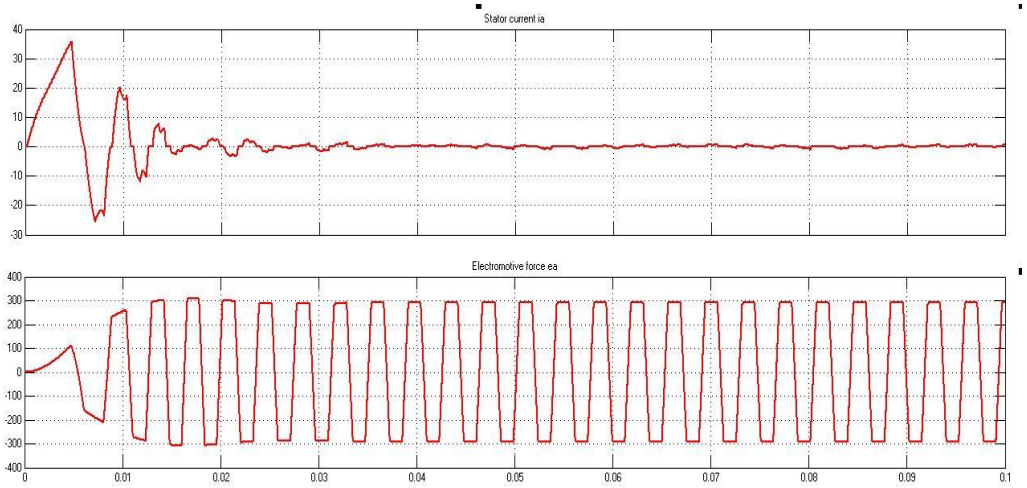

Figure 4:Simulation Stator Current and Electromotive Force waveform of BLDC Motor Drive Fed SEPIC Converter

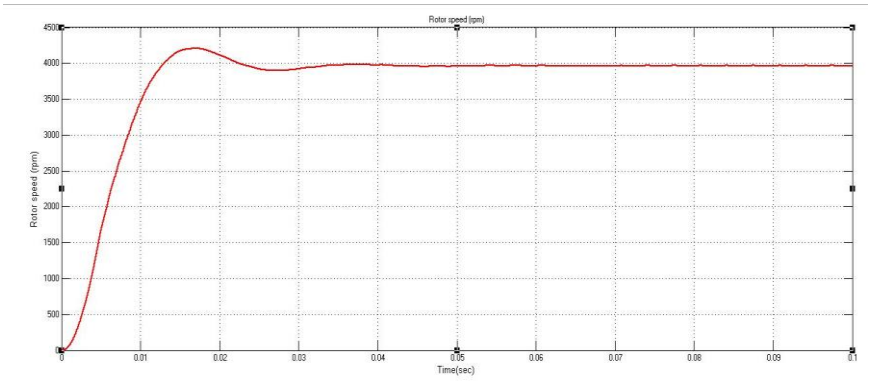

Figure 5:Simulation Rotor Speed waveform of BLDC Motor Drive Fed SEPIC Converter

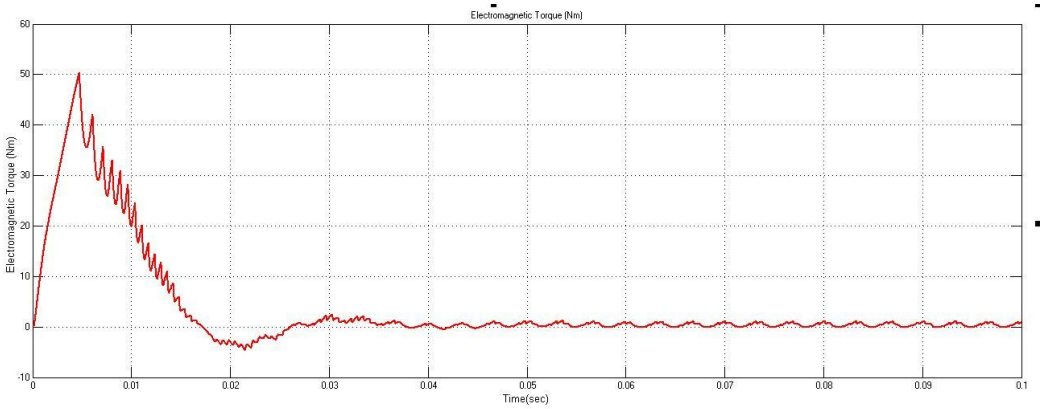

Figure 6:Simulation Torque waveform of BLDC Motor Drive Fed SEPIC Converter

V. Conclusion

This Paper uses a high-voltage gain SEPIC DC-DC converter to further define BLDC driven pumping systems. Good operational data under conditions of constant speed has prompted a detailed evaluation of the proposed work. This study recommends an incredibly fast EV charger. Three separate, single-phase, interleaved, two-module SEPIC-based converters with parallel coupling between their outputs make up the design. Increased system reliability is a result of this design's three primary components: modularity, fault ride-through capabilities, and redundancy.

The simulation for a two-module interleaved system was conducted using MATLAB/Simulink. The Matlab/Simulink environment is used to assess ways to reduce torque ripples, improve the stability index, reduce speed error, and improve power-quality characteristics under different speed conditions. These combined benefits make them more appropriate for pumping applications and very advantageous from a cost standpoint. Reducing harmonics, tightening control of DC output voltage, and boosting source side power factor are examples of improved power-quality features that can be achieved with reasonable implications.

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